CLAIMS

1. A trench-gate semiconductor device, comprising:

a semiconductor body having an active cell area wherein trenches containing gate material extend into the semiconductor body from a surface thereof, wherein adjacent to each trench-gate there is a source region at said semiconductor body surface separated from a drain region by a channel-accommodating body region, and wherein a source electrode contacts the source regions on said semiconductor body surface; characterised in that

the active cell area has a network of connected said trenches with a said source region in each said cell;

trenches containing gate material extend from the network of connected trenches beyond the active cell area to an inactive area where said source regions are not present; and

within said inactive area there is a gate electrode contact area where a gate electrode contacts the gate material on the whole area of the trenches adjacent the semiconductor body surface and where the gate electrode also contacts the semiconductor body surface adjacent the trenches.

2. A semiconductor device as claimed in claim 1, wherein the semiconductor body surface contacted by the gate electrode has first regions at that surface of one conductivity type, said first regions having underlying second regions of opposite conductivity type.

3. A semiconductor device as claimed in claim 2, wherein the source regions in the active cell area and said first regions in the inactive area are of a same first conductivity type, wherein the channel-accommodating body regions in the active cell area and said second regions in the inactive area are of a same second conductivity type opposite to the first conductivity type, and wherein a common layer of the first conductivity type provides the

drain regions in the active cell area and underlies the second regions in the inactive area.

4. A semiconductor device as claimed in claim 3, wherein said first regions and said underlying second regions in the inactive area are provided as isolated cells surrounded by a further network of connected trenches which is an extension of the network of connected trenches in the active cell area.

5. A semiconductor device as claimed in claim 4, modified in that at least some of said isolated cells in the inactive area which are nearest to the active area are instead linking cells across the inactive and active areas, wherein each linking cell has a said first region contacted by the gate electrode, a source region contacted by the source electrode, and a said underlying second region continuous with a said channel-accommodating body region which extends to the semiconductor body surface where it is contacted by the source electrode, the linking cells providing voltage protection diodes between the gate electrode and the source electrode.

6. A semiconductor device as claimed in claim 3, wherein said trenches which extend from the network of connected trenches in the active cell area are stripe shaped trenches which each extend completely across the gate electrode contact area, wherein linking cells are provided across the inactive and active areas between the stripe shaped trenches, wherein each linking cell has a said first region contacted by the gate electrode, a source region contacted by the source electrode, and a said underlying second region continuous with a said channel-accommodating body region which extends to the semiconductor body surface where it is contacted by the source electrode, the linking cells providing voltage protection diodes between the gate electrode and the source electrode.

7. A semiconductor device as claimed in any one of claims 1 to 6, wherein a patterned insulating layer is provided on the semiconductor body, wherein in the active cell area the insulating layer provides an insulating overlayer on the trench-gates and the insulating layer has windows where the source electrode contacts the source regions, and wherein in the inactive area a window in the insulating layer provides the gate electrode contact area.

8. A semiconductor device as claimed in any preceding claim, wherein in the active cell area an insulating layer is provided in the trenches between the gate material in the trenches and the semiconductor body adjacent the trenches.

9. A semiconductor device as claimed in any preceding claim, wherein the gate electrode provides a gate bond pad within the gate electrode contact area.

10. A method of manufacturing a trench-gate semiconductor device, the device comprising:

a semiconductor body having an active cell area wherein trenches containing gate material extend into the semiconductor body from a surface thereof, wherein adjacent to each trench-gate there is a source region at said semiconductor body surface separated from a drain region by a channel-accommodating body region, and wherein a source electrode contacts the source regions on said semiconductor body surface; characterised in that the method includes the steps of:

(a) providing the semiconductor body with a first layer of a first conductivity type suitable for the drain regions and a second layer of a second conductivity type, opposite to the first conductivity type, suitable for the channel-accommodating body regions, the second layer overlying the first layer and extending to the surface of the semiconductor body;

(b) forming a network of connected trenches containing gate material in the active cell area where a said source region will be present in each cell, and at the same time forming trenches containing gate material extending from the network of connected trenches beyond the active cell area to an inactive area where the source regions will not be present in the device, the trenches extending past the second layer and into an underlying portion of the first layer in both the active and inactive areas, and planarising the top surface of the gate material level with the surface of the semiconductor body in both the active and inactive areas;

(c) forming surface regions of the first conductivity type extending into said second layer at the same time in both the active and inactive areas, the source regions being provided by said surface regions of first conductivity type in the active area;

(d) providing a patterned insulating layer on the semiconductor body, the insulating layer providing an insulating overlayer on the trench-gates in the active area, the insulating layer having windows where the source electrode will contact the source regions in the active area, and the insulating layer having a window providing a gate electrode contact area within the inactive area; and

(e) providing a conductive material to form the source electrode contacting the source regions at said insulating layer windows in the active area, and at the same time providing the conductive material to form a gate electrode, the gate electrode contacting the gate material on the whole area of the trenches adjacent the semiconductor body surface at said insulating layer window in the inactive area, and the gate electrode also contacting said surface regions of the first conductivity type at the semiconductor body surface adjacent the trenches at said insulating layer window in the inactive area.

11. A method as claimed in claim 10, wherein said extending trenches are formed in step (b) as a further network of connected trenches

which is an extension of the network of connected trenches in the active cell area, wherein isolated cells surrounded by the further network of connected trenches are provided in the inactive area by the surface regions of the first conductivity type formed in step (c) and underlying regions of the second layer, with the modification that at least some of said isolated cells in the inactive area which are nearest to the active area are instead linking cells across the inactive and active areas, wherein after the provision of the insulating layer in step (d) and the provision of the source and gate electrodes in step (e) each linking cell has a said surface region of the first conductivity type contacted by the gate electrode, a source region contacted by the source electrode, and a region of said second layer underlying said surface region and continuous with a said channel-accommodating body region which extends to the semiconductor body surface where it is contacted by the source electrode, the linking cells providing voltage protection diodes between the gate electrode and the source electrode.

12. A method as claimed in claim 10, wherein said extending trenches are formed in step (b) as stripe shaped trenches which each will extend completely across the gate electrode contact area, wherein linking cells are provided across the inactive and active areas between the striped shaped trenches by the surface regions of the first conductivity type formed in step (c) and underlying regions of the second layer, wherein after the provision of the insulating layer in step (d) and the provision of the source and gate electrodes in step (e) each linking cell has a said surface region of the first conductivity type contacted by the gate electrode, a source region contacted by the source electrode, and a region of said second layer underlying said surface region and continuous with a said channel-accommodating body region which extends to the semiconductor body surface where it is contacted by the source electrode, the linking cells providing voltage protection diodes between the gate electrode and the source electrode.

13. A method as claimed in any one of claims 10 to 12, further including the step of providing an insulating layer in the trenches in the active area and in the inactive area between the gate material in the trenches and the semiconductor body adjacent the trenches.

14. A method as claimed in any one of claims 10 to 13, further including the step of providing a gate bond pad with the gate electrode within the gate electrode contact area.